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PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Ross Addinall  
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CASE 1/3-1/2

TITLE Improvements In Or Relating To Integrated Circuit Dies

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NEW APPLICATION UNDER 37 CFR § 1.53(b)

Enclosed are the following papers relating to the above-named application for patent:

Specification  
2 Formal Sheets of drawing(s)  
Declaration and Power of Attorney  
Information Disclosure Statement  
Certified Copy of European Patent Application No. 99306444.3  
Certified Copy of European Patent Application No. 99309842.5

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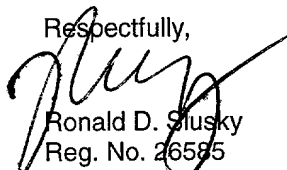
CLAIMS AS FILED				
	NO. FILED	NO. EXTRA	RATE	CALCULATIONS
Total Claims	15 - 20 =	0	x \$18 =	\$0
Independent Claims	2 - 3 =	0	x \$78 =	\$0
Multiple Dependent Claims, if applicable			+ \$260 =	\$260
Basic Fee				\$690
			<b>TOTAL FEE</b>	<b>\$950</b>

Please file the application and charge **Lucent Technologies Deposit Account No. 12-2325** the amount of \$950, to cover the filing fee. Duplicate copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 12-2325** as required to correct the error.

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09639288-081500

## IMPROVEMENTS IN OR RELATING TO INTEGRATED CIRCUIT DIES

### Cross-Reference To Related Application

This application claims priority of European Patent Application No. 99306444.3, which was filed on August 17, 1999 and European Patent Application No. 99309842.5 which was filed on December 07, 1999.

### 5 Field Of The Invention

This invention relates to integrated circuit dies.

### Background Of The Invention

When an integrated circuit design nears the production stage it is usual to produce a prototype version having additional conductive pads to which connection may be made  
10 for testing and de-bugging purposes. Where conventional wire bonding is used to make connections to the pads on the integrated circuit die, it is common practice to provide a plurality of conductive pads to all of which wire bond connections may be made for testing and de-bugging purposes and to a subset of which wire bond connections may be made in final production. However in the case of an integrated circuit die which will be  
15 assembled as a so-called flip-chip it is necessary for the center-to-center pitch, or spacing, between the conductive pads to be much larger than is necessary where wire bonding is used to make the connections. This much larger pitch renders it impractical to adopt the same idea as in the wire bonding case, that is having additional pads for testing and de-bugging, because the integrated circuit die would be so large that it would be  
20 uneconomic.

### Summary Of The Invention

According to this invention an integrated circuit die includes first and second sets of conductive pads for enabling external connections to be made to the integrated circuit, there being at least a first predetermined center-to-center spacing between each pad of the  
25 first set and the adjacent pad or pads of the first set, and at least a second predetermined center-to-center spacing, less than said first spacing, between each pad of the second set and the adjacent pad or pads of the first and second sets, and a passivation layer exposing only pads of the first set, or exposing pads of the first and second sets.

The pads of the first set may be larger in area than the pads of the second set. The area of each pad of the first set and the first predetermined center-to-center spacing may be suitable for flip-chip assembly of the die, and the area of each pad of the second set and the second predetermined center-to-center spacing may be suitable for wire bond  
5 assembly of the die.

The pads of the first and second sets may be disposed in-line adjacent one or more edges of the die.

The pads of the first set may be disposed in two lines adjacent one or more edges of the die, the pads of the first set in one of the two lines being disposed in staggered  
10 relationship with respect to the pads of the first set in the other of the two lines. The pads of the second set may be disposed in one of the two lines.

The first set of pads may be connected to one set of connection points in the integrated circuit, and the second set of pads may be connected to another set of connection points in the integrated circuit.

15 **Brief Description Of The Drawings**

The invention will now be described by way of example with reference to the accompanying drawings, in which:

FIG.1 is a schematic cross section of part of an integrated circuit die embodying the invention;

20 FIG.2 is a schematic cross section of part of an integrated circuit die embodying the invention; and

FIG.3 is a schematic plan view of part of an integrated circuit die embodying the invention.

In the various figures, which are not to scale, like references denote like parts.

25 **Detailed Description**

Referring now to Fig.1, an integrated circuit die comprises polysilicon and metal layers shown schematically at 1 and making up the circuitry (not shown) embodied in the integrated circuit. Deposited on the surface of 1 is a first set of conductive pads 2 and a second set of conductive pads 3. The sets of conductive pads 2 and 3 are provided for the  
30 purpose of enabling connection to be made between the circuitry embedded in the integrated circuit and external terminals (not shown). The first set of pads 2, which are

considerably larger than the second set of pads 3, are provided for flip-chip assembly as will be described later, and are connected (by means not shown) to one set of connection points in the circuitry. The second set of pads 3 are provided to enable wire bond connections to be made to the integrated circuit e.g. for testing and de-bugging purposes, and are connected (by means not shown) to another set of connection points in the circuitry. Wire bond connections may also be made to the first set of pads 2, and, as shown, all of the pads 2 and 3 have a wire bond connection 4 thereto. A passivation layer 5 of conventional passivating material is provided over the surface of the integrated circuit die leaving an area uncovered on each of the pads 2 and 3 for the wire bond connections 4 thereto. The pitch, or center-to-centre spacing, between each pad 2 of the first set and the adjacent pad or pads 2 of the first set is at least a predetermined amount required for flip-chip assembly. Currently this pitch is 200 microns or 250 microns depending on the manufacturer. A smaller pitch than that required will result in manufacturing problems and a significant rejection rate. The minimum pitch for connection by wire bonding is much less and is currently 90 microns, although with present wire bonding technology the pitch could be as low as 50 microns. Thus the center to center spacing, or pitch, between each pad 3 of the second set of pads and the adjacent pad or pads, whether it be a pad 2 of the first set of pads or a pad 3 of the second set of pads, must be at least equal to the lower spacing requirements imposed by wire bonding.

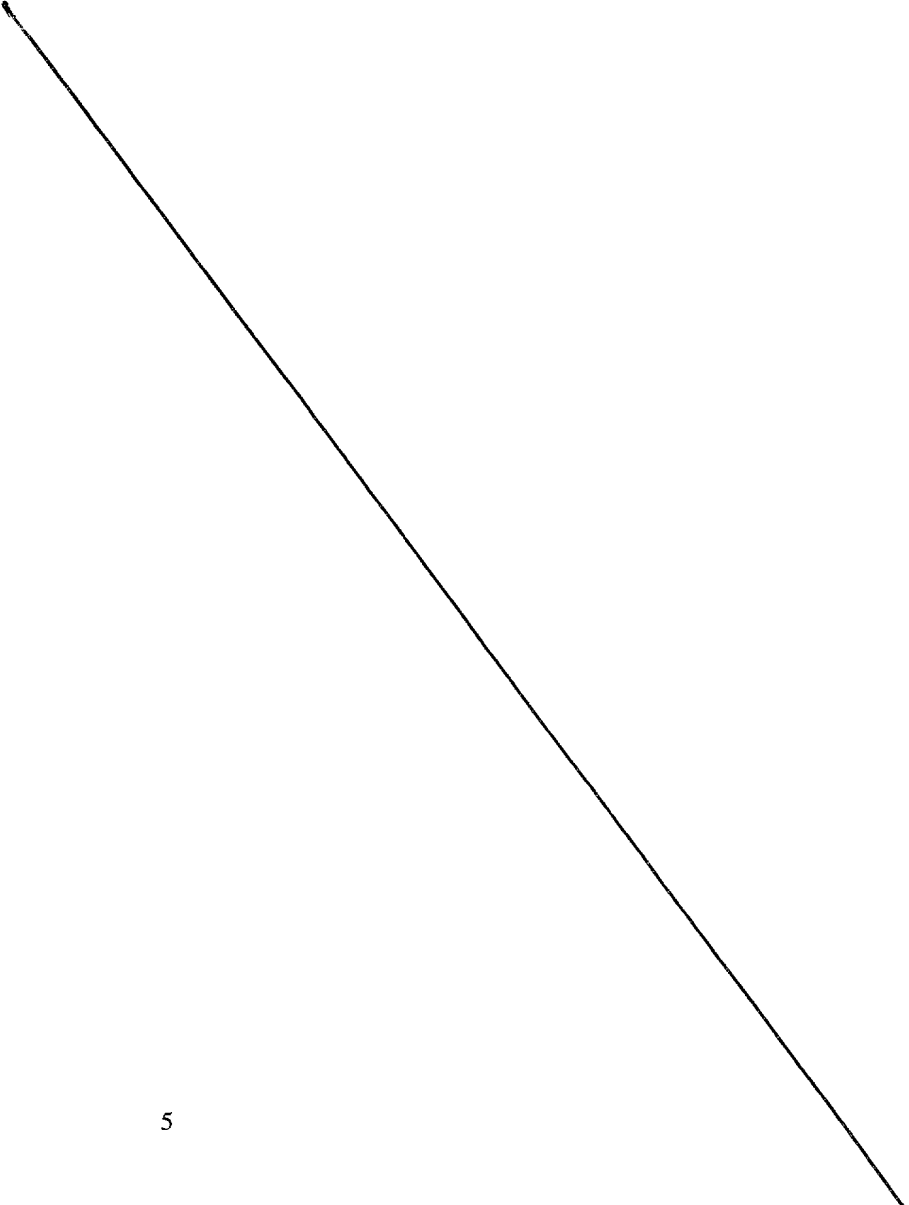
Fig.2 shows the same basic integrated circuit die shown in Fig.1 but, instead of the passivating layer 5 of Fig.1 exposing the conductive pads for wire bond connections thereto, Fig.2 shows the integrated circuit die prepared for flip-chip assembly. To this end, a passivating layer 6 is provided over the surface of the die exposing only the pads 2 of the first set of pads which, as previously noted with reference to Fig.1, are of a size suitable for flip-chip assembly. It will be noted that passivating layer 6 exposes an area of pads 2 which is greater than for the wire bond assembly case shown in Fig.1. Each of the pads 2 has deposited thereon a "bump" of conductive material, such as gold or solder, which by the application of heat is caused to re-flow and effect connection between its respective pad 2 and an external terminal (not shown). The mechanics of flip-chip assembly are well known and will not be described further. Because passivating material

6 covers the conductive pads 3 of the second set, the necessary minimum pitch imposed by flip-chip assembly between each conductive pad 2 and the pad or pads adjacent thereto is ensured. If the pads 3 of the second set of pads were not covered by passivating material 6 the minimum pitch requirements for flip-chip assembly would not  
5 be met, and problems during such assembly would be likely with a significant rejection rate of assembled dies.

It will be appreciated that an integrated circuit die embodying the invention may simultaneously comply with the minimum pitch requirements for both flip-chip assembly and wire bonding without any, or any significant, increase in the size of the die. Thus the  
10 same die may be used in a flip-chip assembly process or a conventional wire bonding assembly process merely by changing a single mask layer namely, the passivation layer.

The invention is not limited in its application to in-line pads. For example, two rows of pads may be provided as long as the minimum pitch requirements for flip-chip assembly and wire bonding are satisfied. Fig.3 shows in schematic plan view part of an  
15 integrated circuit die having two rows of pads. As in Figs. 1 and 2, two sets of pads are shown, the first set comprising pads 2' and 2'', and the second set comprising pads 3'. The pads 2' and 3' are arranged in a row or line adjacent to the die edge shown in Fig.3. The pads 2'' are arranged in another row or line parallel with the die edge but further therefrom. The pads 2'' may be, and as shown are, staggered in relation to the other pads  
20 2' of the first set of pads. The pads of the first set, pads 2' and pads 2'', are larger than the pads 3' of the second set of pads and, as in Figs. 1 and 2, the larger pads may be used for flip-chip or wire bonding assembly, whereas the smaller pads 3' are intended for wire bonding assembly. As before, each of pads 2' and 2'' are pitched apart by at least the minimum required distance for flip-chip assembly, the distance being indicated  
25 schematically for two of the staggered pads by the dashed-arrowed line P. Each of the pads 3' of the second set of pads is spaced apart from the adjacent pad or pads, whether of the first or second sets of pads, by at least the minimum spacing required for wire bonding assembly. Staggering of the pads 2' and 2'' has the advantage that the periphery of the die may be reduced and, where these pads are used for wire bond assembly, it also  
30 has the advantage that their effective pitch, i.e. the pitch as measured along the die edge, matches more closely the pitch of the lead frame of an intended package.

It will be appreciated that the spacing between the pads in Figs. 1, 2 and 3 need not be uniform or symmetrical; what is required is that the spacing between each pad and the adjacent pad or pads be at least the required minimum spacing for flip-chip or wire bond assembly as the case may be.

- 5        The invention permits the same basic integrated circuit die to be used for flip-chip production, and a higher pin count version to be produced for wire bonding. Such a “dual purpose” die may be produced without an increase in die size. In effect the invention permits two separate integrated circuit dies to be produced at a minimum extra cost. Furthermore, the delay characteristics of the input/output paths and the internal
- 10 parasitic characteristics of the die are substantially the same for both flip-chip and wire bonding assembly options. As will be appreciated, the invention permits the decision as to whether to use flip-chip or wire bonding assembly to be made at a later stage in the production cycle.
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## CLAIMS

1           **1.** An integrated circuit die including first and second sets of conductive pads for  
2 enabling external connections to be made to the integrated circuit, there being at least a  
3 first predetermined center-to-center spacing between each pad of the first set and the  
4 adjacent pad or pads of the first set, and at least a second predetermined center- to-center  
5 spacing, less than said first spacing, between each pad of the second set and the adjacent  
6 pad or pads of the first and second sets, and a passivation layer exposing only pads of the  
7 first set, or exposing pads of the first and second sets.

1           **2.** A die as claimed in claim 1 wherein the pads of the first set are larger in area  
2 than the pads of the second set.

1           **3.** A die as claimed in claim 2 wherein the area of each pad of the first set and the  
2 first predetermined center-to-center spacing are suitable for flip-chip assembly of the die,  
3 and the area of each pad of the second set and the second predetermined center-to-center  
4 spacing are suitable for wire bond assembly of the die.

1           **4.** A die as claimed in claim 1 wherein the pads of the first and second sets are  
2 disposed in line adjacent one or more edges of the die.

1           **5.** A die as claimed in claim 1 wherein the pads of the first set are disposed in two  
2 lines adjacent one or more edges of the die, the pads of the first set in one of the two  
3 lines being disposed in staggered relationship with respect to the pads of the first set in  
4 the other of the two lines.

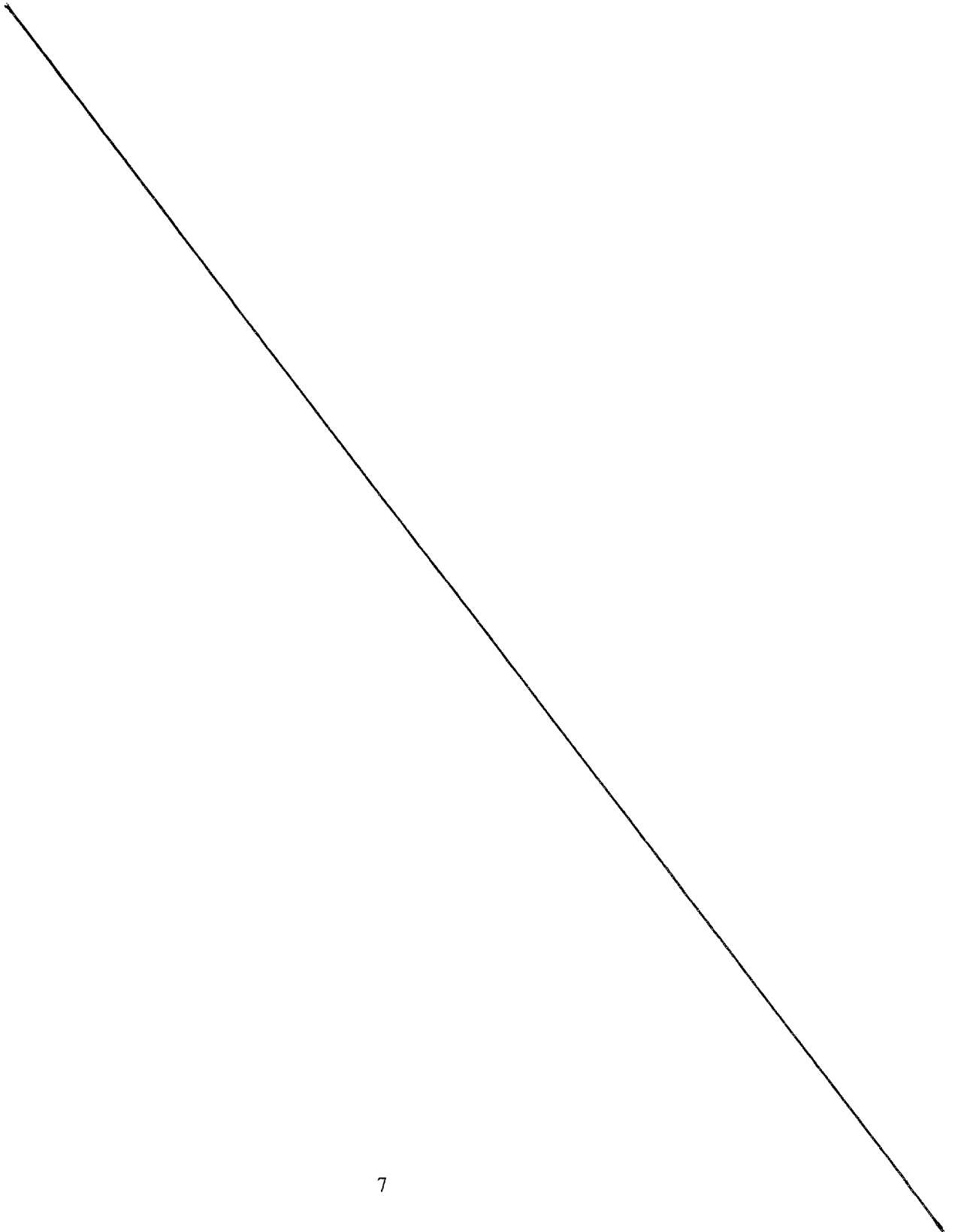
1           **6.** A die as claimed in claim 5 wherein the pads of the second set are disposed in  
2 one of the two lines.

1           7. A die as claimed in any preceding claim wherein the first set of pads is  
2 connected to one set of connection points in the integrated circuit, and the second set of  
3 pads is connected to another set of connection points in the integrated circuit.

1           **8.** An integrated circuit die, comprising:  
2           a first set of conductive pads having a first minimum distance therebetween; and  
3           a second set of conductive pads having a second minimum distance therebetween,  
4   and between a pad of the second set and a neighboring pad of the first set,  
5           wherein the die is adapted for selective use as one of a flip-chip assembly and a  
6   wire bond assembly.

1           **9.** A die as recited in claim 8, further comprising a first passivation layer for use  
2 of the die as a flip-chip assembly.

1           **10.** A die as recited in claim 8, further comprising a second passivation layer for  
2 use of the die as a wire bond assembly.



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## ABSTRACT

An integrated circuit die carries conductive pads and thereon, the larger pads being suitable for flip-chip assembly and the smaller pads being suitable for wire bond assembly. The pitch between pads is at least the minimum required for flip-chip assembly, whereas the pitch between each of pads and the adjacent pad or pads is at least the minimum required for wire bond assembly. For wire bond assembly a passivation layer exposing all pads is provided, whereas for flip-chip assembly a passivation layer exposes only certain pads so that conductive bumps may be provided. The provision of pads complying with the minimum spacing requirements for both flip-chip and wire bond assembly enables a “dual purpose” (e.g. one set of pads being for normal production and another set for testing purposes) die to be produced without any increase in die size.

FIG. 1

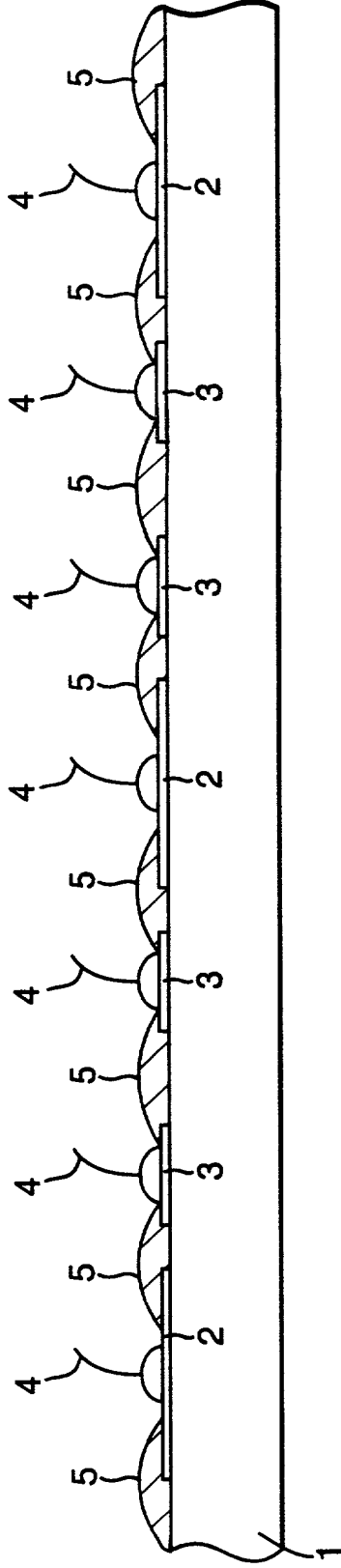


FIG. 2

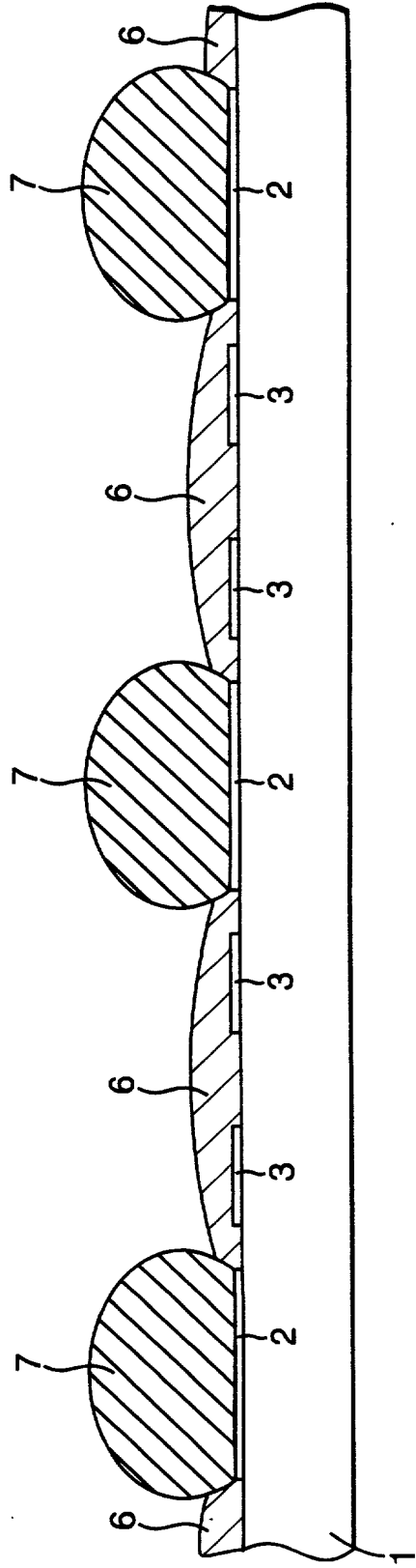
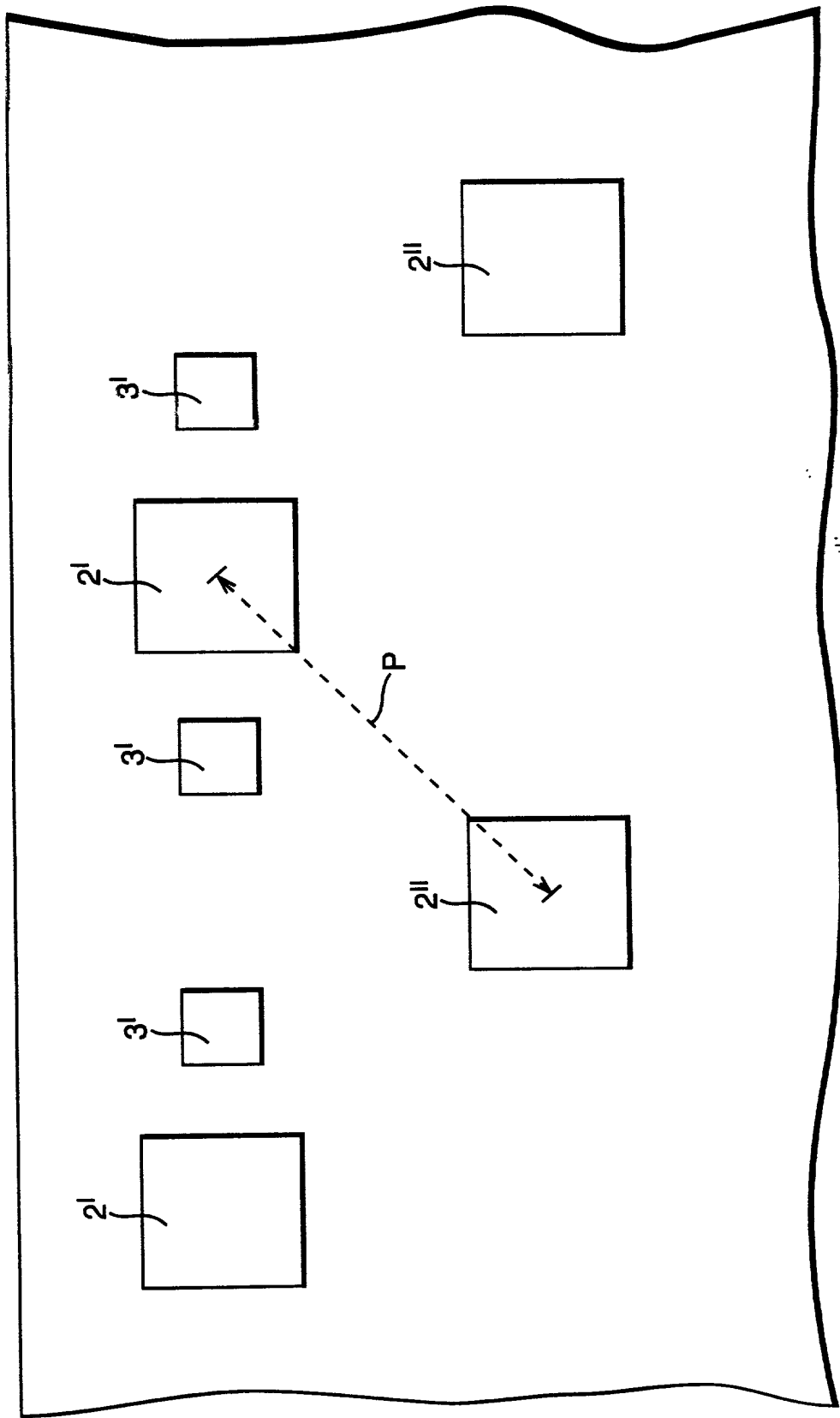


FIG. 3



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Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **Improvements in or relating to integrated circuit dies** the specification of which

[ X ] is attached hereto

OR

[ ] was filed on \_\_\_\_\_ and granted Application Serial Number \_\_\_\_\_.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

**99306444.3    August 17, 1999    and    99309842.5    December 7, 1999**

I hereby claim the benefit under Title 35, United States Code, 120 of any foreign application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

096309842.5-081500

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005760-8826E960

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